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EXAMINER	
EHNE, CHARLES	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,053	LEMPEL ET AL.	
	Examiner	Art Unit	
	Charles Ehne	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *2-4,7 and 16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,6,8-15 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1,5,6,8-11,13-15 and 17-24 are rejected under 35 U.S.C. 103(a) as being anticipated over Arndt (US 2003/0023932) taken in view of Godiwala (5,361,267).

As to claim 1, Arndt discloses a method comprising:

fetching data from a cache in a computer (Page 2, ¶ 0021, lines 1-2);

during the fetching, detecting a soft error in the data (Page 1, ¶ 0004, lines 21-22 & Page 3, ¶ 0028, lines 1-2);

as a result of detecting the soft error, stalling the computer (Page 2, ¶ 0023, lines 8-10);

invoking soft error handler logic to perform invalidating a cache line;(Page 3, ¶ 0026, lines 5-15); and

resuming fetching of the data (Page 3, ¶ 0030, lines 15-16).

Arndt fails to disclose invoking a soft error handler logic to perform on of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache.

Godiwala discloses a cache policy wherein any dirty cache entry that is to be victimized as a result of a read operation is flushed from the cache (column 48, lines 1-5). Godiwala does disclose wherein invoking a soft error handler logic to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache (column 47, lines 30-34).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Godiwala's method to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache with Arndt's method of handling soft errors. A person of ordinary skill in the art would have been motivated to make the modification because by only clearing one cache line would require less space in the main memory than clearing the entire cache (column 46, lines 24-27).

As to claim 5, Arndt discloses the method of claim 1, wherein the error is detected by comparing an expected parity of the cache line with a calculated parity of the cache line (Page 3, ¶ 0028, lines 1-2).

As to claim 6, Arndt discloses a system comprising:

a memory (Page 1, ¶ 0015, lines 12-13);

a processor coupled to the memory (Page 2, ¶ 0016, lines 5-7);

a cache coupled to the processor (Page 2, ¶ 0021, lines 1-2);

soft error detection logic coupled to the cache to detect soft errors therein (Page 1, ¶ 0009, lines 1-4 & Page 3, ¶ 0028, lines 1-2); and

soft error handling decision logic coupled to the soft error detection logic invoke soft error handler logic based on an input from the soft error detection logic (Page 3, ¶ 0026, lines 5-15).

Arndt fails to disclose a soft error handler logic to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediated portion of the cache.

Godiwala discloses a cache policy wherein any dirty cache entry that is to be victimized as a result of a read operation is flushed from the cache (column 48, lines 1-5). Godiwala does disclose a soft error handler logic to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediated portion of the cache (column 47, lines 30-34).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Godiwala's method to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache with Arndt's method of handling soft errors. A person of ordinary skill in the art would have been motivated to make the modification because by only clearing one cache line would require less space in the main memory than clearing the entire cache (column 46, lines 24-27).

As to claim 8, Arndt discloses the system of claim 6, further comprising a soft error recovery memory to store information associated with recovering from a soft error (Page 3, ¶ 0028, lines 2-7).

As to claim 9, Arndt discloses the system of claim 8, wherein the information is an address of a cache line containing a soft error (Page 3, ¶ 0024, lines 4-7).

As to claim 10, Arndt discloses the system of claim 8, wherein the soft error recovery memory comprises a register (Page 3, ¶ 0028, lines 2-7).

As to claim 11, Arndt discloses the system of claim 6, wherein the soft error detection logic is to compare an expected parity of a cache line with a calculated parity of the cache line (Page 3, ¶ 0028, lines 1-2).

As to claim 13, Arndt discloses a processor comprising:

a cache (Page 2, ¶ 0021, lines 1-2);

soft error detection logic coupled to the cache (Page 1, ¶ 0009, lines 1-4 & Page 3, ¶ 0028, lines 1-2); and

decision logic to receive at least first, second and third input values (Page 3, ¶ 0028, line 7), the first input value being a request to invoke a soft error handler (Page 3, ¶ 0028, lines 1-7), the second input value corresponding to data in a cache line of the instruction cache (Page 3, ¶ 0028, lines 2-7), and the third input value being an indicator from the soft error detection logic to indicate whether a soft error is present in the data in the cache line (Page 3, ¶ 0029, lines 1-3).

Arndt fails to disclose invoking a soft error handler logic to perform on of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache.

Godiwala discloses a cache policy wherein any dirty cache entry that is to be victimized as a result of a read operation is flushed from the cache (column 48, lines 1-5). Godiwala does disclose wherein invoking a soft error handler logic to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache (column 47, lines 30-34).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Godiwala's method to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache with Arndt's method of handling soft errors. A person of ordinary skill in the art would have been motivated to make the modification because by only clearing one

cache line would require less space in the main memory than clearing the entire cache (column 46, lines 24-27).

As to claim 14, Arndt discloses the processor of claim 13, further comprising a register to store an address of a cache line containing data currently being fetched (Page 3, ¶ 0024, lines 4-7).

As to claim 15, Arndt discloses the processor of claim 13, wherein the soft error detection logic is to compare an expected parity of the data, and a calculated parity of the data (Page 3, ¶ 0028, lines 1-2).

As to claim 17, Arndt discloses the method of claim 1, further comprising:

After detecting the soft error, storing the address of the cache line corresponding to the at least one instruction in a register; and issuing a request to a soft error handler to clear the soft error (Page 3, ¶ 0028, lines 2-7).

As to claim 18, Arndt discloses the method of claim 17, wherein the soft error handler:

stops fetching of instructions from the cache (Page 3, ¶ 0029, lines 1-3);

reads the address in the register (Page 3, ¶ 0024, lines 4-7 & ¶ 0025, lines 3-10); and

clears the corresponding cache line (Page 3, ¶ 0033, lines 1-3).

As to claim 19, Arndt discloses the method of claim 17, further comprising resuming execution of the sequence of computer instructions at the instruction corresponding to the cleared cache line (Page 4, ¶ 0030, lines 15-17).

As to claim 20, Arndt discloses a machine-readable medium storing computer-executable instructions which, when executed by a processor, implement a process according to claim 1(see claim 1 rejection).

As to claim 21, Arndt discloses the machine-readable medium of claim 20, the process further including reading a memory storing an address of the cache line (Page 3, ¶ 0028, lines 9-10).

As to claim 22, Arndt discloses the machine-readable medium of claim 20, the process further including invalidating the cache line (Page 3, ¶ 0033, lines 1-3).

As to claim 23, Arndt discloses an apparatus comprising:

a cache (Page 2, ¶ 0021, lines 1-2);

a comparator coupled to the cache to compare a calculated parity bit and an expected parity bit, the comparator including an output coupled to an enable input of a recovery register, the enable input to cause the recovery register to store an address of a cache line identified as containing a soft error (Page 3, ¶ 0028, lines 1-3); and

Arndt does not disclose a selector coupled to the cache line, to select on of a soft error handler request or the cache line based on the comparator output, the soft error handler request to invoke a soft error handler, the soft error handler to receive the address of the cache line identified as containing a soft error from the recovery register, and to perform one of the multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache.

Godiwala discloses a cache policy wherein any dirty cache entry that is to be victimized as a result of a read operation is flushed from the cache (column 48, lines 1-5). Godiwala does disclose a selector coupled to the cache line, to select on of a soft error handler request or the cache line based on the comparator output, the soft error handler request to invoke a soft error handler, the soft error handler to receive the address of the cache line identified as containing a soft error from the recovery register, and to perform one of the multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache (column 47, lines 30-34 & lines 44-52).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Godiwala's method to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache based on the output with Arndt's method of handling soft errors. A person of ordinary skill in the art would have been motivated to make the modification because by only clearing one cache line would require less space in the main memory than clearing the entire cache (column 46, lines 24-27).

As to claim 24, Arndt discloses an apparatus of claim 23, wherein the soft error handler comprises microcode (Page 3, ¶ 0028, lines 1-2).

Claim 12 is rejected under 35 U.S.C. 103(a) as being anticipated over Arndt taken in view of Bossen (6,332,181).

As to claim 12, Arndt discloses a system comprising: soft error detection logic coupled to the cache to detect soft errors therein; soft error handling decision logic coupled to the soft error detection logic to perform one of a plurality of operations based on an input from the soft error detection logic; and a soft error handler invokable by the soft error handling decision logic to perform one of operations to clear the soft error. However Arndt fails to disclose wherein the soft error handling decision logic comprises a multiplexer to select as input one of data corresponding to a cache line currently being fetched and request to invoke the soft error handler, depending on a value of an output of the soft error detection logic.

Bossen disclose a system of handling cache errors which invokes a recovery upon reporting the error (Abstract, lines 1-2). Bossen does disclose wherein the soft error handling decision logic comprises a multiplexer to select as input one of data corresponding to a cache line currently being fetched and request to invoke the soft error handler, depending on a value of an output of the soft error detection logic (Figure 2, columns 4-5, lines 67-14).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement Bossen's multiplexer with Arndt's detection signal and corresponding fetched data. A person of ordinary skill in the art would have been motivated to make the modification because the multiplexer outputs the data containing the error to an appropriate error handler based upon the presence of an error signal (Bossen: column 5, lines 3-14).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Ehne whose telephone number is (571)-272-2471. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.